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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,602	12/29/2003	Chang Hun Han	20063/10017	6477
34431	7590	11/21/2005	EXAMINER	
HANLEY, FLIGHT & ZIMMERMAN, LLC			JEFFERSON, QUOVAUNDA	
20 N. WACKER DRIVE			ART UNIT	
SUITE 4220			PAPER NUMBER	
CHICAGO, IL 60606			2823	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/747,602

Applicant(s)

HAN ET AL.

Examiner

Quovaunda Jefferson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>29 December 2003</u> <u>25 March 2004</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The applicant discloses the forming a sidewall oxide layer on the resultant substrate. Using the term "sidewall oxide layer" would give one that is skilled in the art the impression that this layer is only formed or deposited on the sidewall spacers of the substrate or that the applicant is referring to the sidewall spacers, since sidewall spacers can be formed from an oxide layer. Yet, the applicant shows in the drawings that this "sidewall oxide layer" is indeed deposited on the entire surface of the substrate

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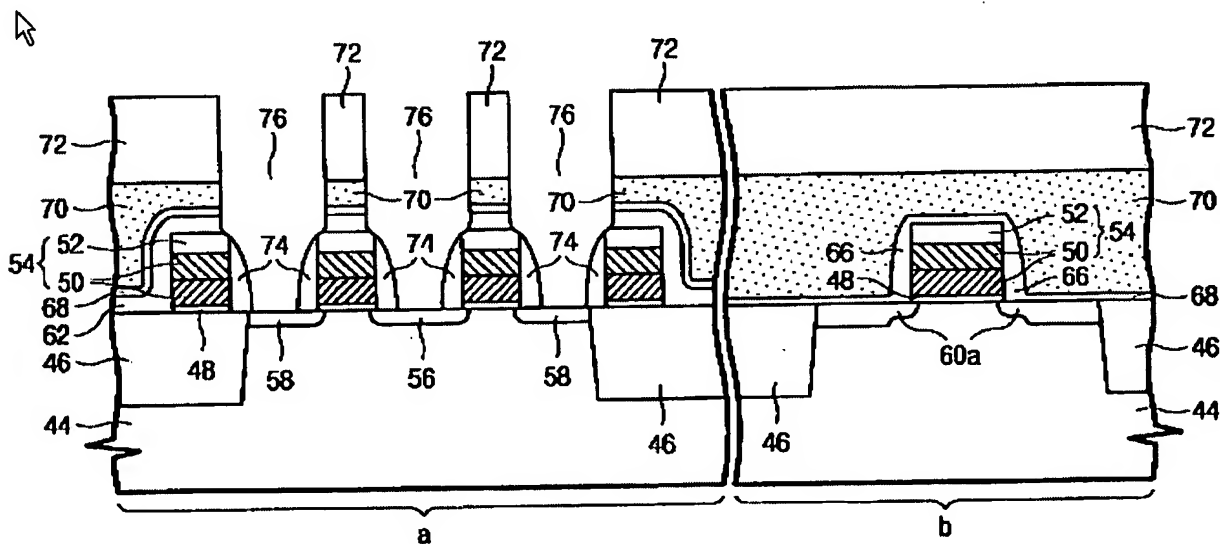
and not just the sidewall spacers. Applicant is required to change the term of "sidewall oxide layer".

Claim Rejections - 35 USC § 103

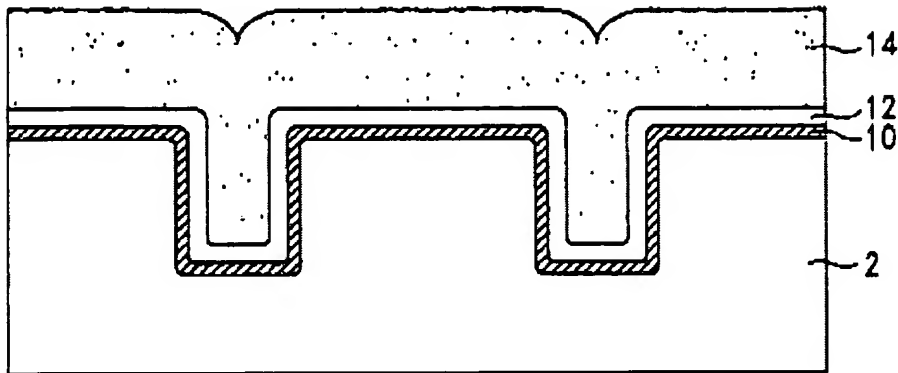
The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al, US Patent 6,417,097 and Wu, US Patent 6,156,854.



Hwang, Figure 6A



Wu, Figure 6

Regarding claim 1, Hwang teaches a method for fabricating a semiconductor device comprising of forming a gate oxide **48** and a gate electrode **50** on a semiconductor substrate, performing a first ion implantation process for the formation of a (lightly doped drain) LDD region **60a** in the substrate, forming spacers **66**, **74** on the sidewalls of the gate electrode, performing a second ion implantation process for the formation of a junction region **58**, **60a** in the substrate using the spacers as a mask, forming a trench **46** for device isolation by removing selectively the top portion of the substrate between the spacers, planarizing the gap filling insulating layer **70**, and removing selectively some part of the gap filling insulation layer to form contact holes **76**. See Hwang, figure 6A

Hwang fails to teach forming a sidewall oxide layer on the resulting substrate, forming a diffusion barrier on the sidewall oxide layer, and depositing a gap filling insulation layer over the diffusion barrier. Wu teaches forming a sidewall oxide layer **10**

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on the resulting substrate, forming a diffusion barrier **12** on the sidewall oxide layer, and depositing a gap filling insulation layer **14** over the diffusion barrier. It would have been obvious to one skilled in the art to combine the teachings of Wu and Hwang because for CMOS technology, an effective device isolation method that provides abrupt transitions to active device regions with minimum impact on device characteristics or topography will be required (column 1, lines 60-63). See Wu, figure 6.

Regarding claim 2, Wu further teaches a method as defined by claim 1, wherein the gap filling insulation layer is formed of boro-phosphosilicate glass (BPSG) (column 4, line 32).

Regarding claim 4, Wu teaches a method as defined by claim 1, wherein the diffusion barrier is an N-doped oxide layer (column 4).

Regarding claim 5, Wu further teaches a method as defined by claim 1, wherein the gap filling insulation layer is formed of undoped silicate glass (USG) (column 4, line 34).

Regarding claim 6, Hwang further teaches a method as defined by claim 1, wherein the gap filling insulation layer is used as both a device isolation layer and an interlayer insulation layer.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang and Wu as applied to claim 1 above, and further in view of Chen, US Patent 5,597,747. While Wu and Hwang fail to teach a method as defined by claim 1, wherein the diffusion barrier is formed of amorphous silicon, Chen teaches the diffusion barrier is formed of amorphous silicon (column 1, line 16). It would have been obvious to combine the teachings of Chen with that of Hwang and Wu because this allows a gap to be etched in the N+ silicon that is perfectly aligned with the gate electrode (abstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qvj



W. DAVID COLEMAN
PRIMARY EXAMINER